United Monolithic Semiconductors

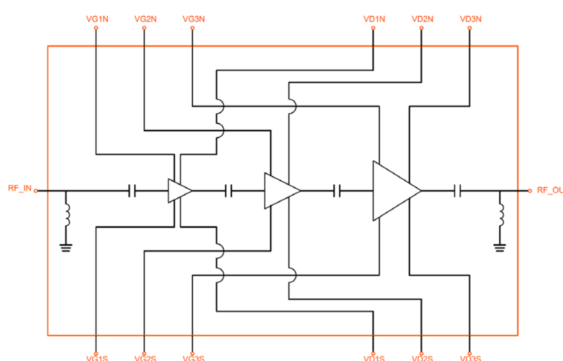
CHA8262-99F

27.5 - 31.5 GHz 12W HPA

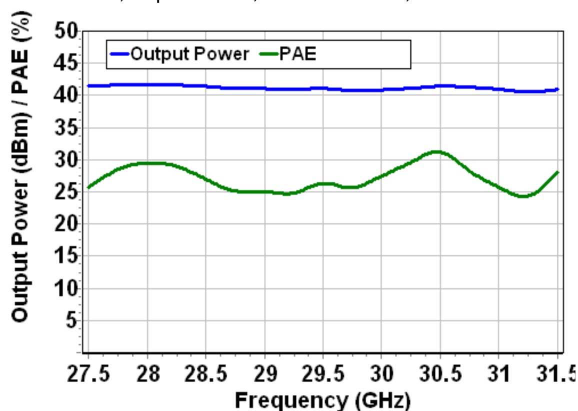
GaN Monolithic Microwave IC bare die

Description

The CHA8262-99F is a three stage monolithic GaN High Power Amplifier reaching 12W Output Power over 27.5-31.5GHz bandwidth.
It offers high linearity performances and reaches more than 25% of Power Added Efficiency at saturation. The circuit is manufactured on a 0.15µm gate length GaN-on-SiC HEMT process and is available in bare die form.
It is well suited for SatCom uplink and 5G communication applications.



Vd = +20V, Idq = 280mA, Pin = 20.5dBm, Tcase = 25°C



Main Features

- 27.5 – 31.5GHz Frequency Range
- Linear Gain is 24dB
- Pout > 41dBm @ Pin = 23.5dBm
- PAE > 25% @ Psat
- DC bias: Vd=20V @ Idq=280mA

Main Electrical Characteristics

Tcase = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.5		31.5	GHz
Gain	Linear Gain		24		dB
Psat	Saturated Output Power		41		dBm
PAE	Power Added Efficiency		25		%
Idq	Total quiescent bias drain current		280		mA
Tcase	Operating temperature range at MMIC backside level	-40		105	°C

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
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Specifications

Tcase = +25°C, Vd = +20V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.5		31.5	GHz
Gain	Linear Gain		24		dB
Psat	Saturated Output power		41		dBm
Pae	Power Added Efficiency		25		%
S11	Input Return Loss		-10		dB
S22	Output Return Loss		-8		dB
Idq	Total quiescent drain current		280		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation board".

Absolute Maximum Ratings (1)

Tcase = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Id	Drain bias current	3.5	A
Vg	Gate bias voltage	-6 to -1	V
Pin	Input Power	30	dBm
Tj	Maximum Junction temperature (2)	200	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) See Device thermal performances section

Recommended Operating Range (3), (4)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18 to 25	V
Id	Quiescent Drain bias current	150 to 350	mA
Vg	Gate bias voltage	-3.5 to -2.5	V
Pin	Maximum input Power	27	dBm
Tj	Maximum Junction temperature (2)	200	°C

(3) Electrical performances are defined for specified test conditions

(4) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Tcase	Operating temperature range at MMIC backside level	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

Tcase=+25°C

Symbol	Pad N°	Parameter	Values	Unit
VG1N	2	First stage north gate voltage	~ -3.1	V
VG1S	26	First stage south gate voltage	~ -3.1	V
VG2N	4	Second stage north gate voltage	~ -3.1	V
VG2S	24	Second stage south gate voltage	~ -3.1	V
VG3N	6	Third stage north gate voltage	~ -3.1	V
VG3S	22	Third stage south gate voltage	~ -3.1	V
VD1N	8	First stage north drain voltage	20	V
VD1S	20	First stage south drain voltage	20	V
VD2N	10	Second stage north drain voltage	20	V
VD2S	18	Second stage south drain voltage	20	V
VD3N	12	Third stage north drain voltage	20	V
VD3S	16	Third stage south drain voltage	20	V

“Power ON” sequence

1. Ground the device
2. Set the gate voltages to -5V
3. Increase the drain voltages to 20V
4. Increase the gate voltages to get total drain current of 280 mA
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

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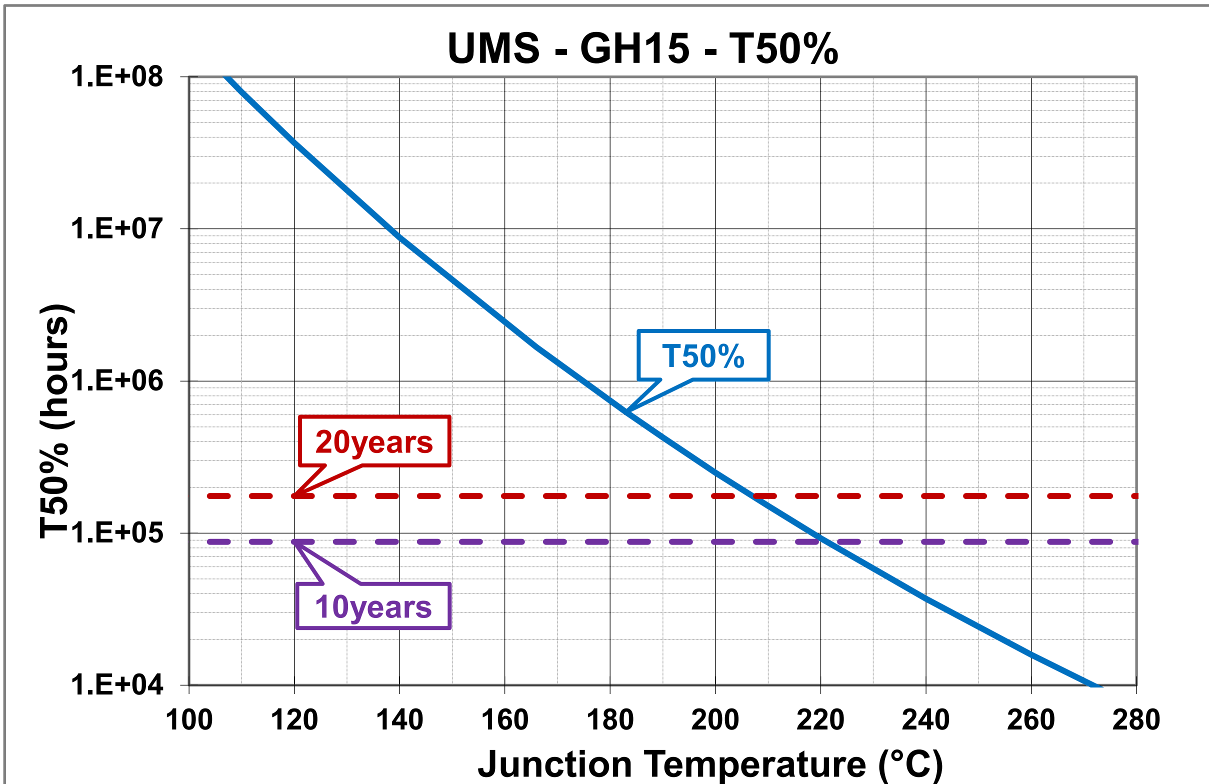
Device thermal performances

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
The temperature is monitored at the MMIC backside interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	RTH (°C/W)	T50 (hours)
RTH [1] Thermal Resistance (Junction to Backside)	Vd=20V Pdiss= 28.6W CW	168	2.9	1.67E+6
RTH [2] Thermal Resistance (Junction to Backside)	Vd=20V Pdiss= 24.9W CW	183	3.1	6.24E+5

[1] Assuming 85°C Tcase
[2] Assuming 105°C Tcase



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Typical On Wafer Sij parameters

Tbackside=+25°C, Vd = +20V, Id = 280mA, Pulsed signal (25µs pulse, 10% width)

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.2	172.4	-78.9	-18.3	-63.6	-143.0	0.0	173.8
2	-0.3	164.6	-68.7	-160.7	-62.4	-144.4	0.0	167.6
3	-0.3	156.8	-89.8	-1.4	-66.5	58.8	-0.1	160.8
4	-0.3	148.7	-74.5	71.4	-66.9	-39.7	-0.1	154.5
5	-0.3	140.4	-87.2	-173.2	-73.4	-142.7	-0.2	147.6
6	-0.4	131.9	-79.0	-152.5	-67.0	100.5	-0.1	139.9
7	-0.4	122.5	-77.8	-119.9	-63.6	151.3	-0.2	131.5
8	-0.4	113.0	-74.7	-78.1	-57.0	93.4	-0.2	120.8
9	-0.5	102.4	-71.2	138.4	-57.8	-113.6	-0.4	105.3
10	-0.5	90.6	-64.2	-73.9	-57.5	-171.1	-1.2	71.1
11	-0.6	77.8	-68.7	-148.7	-60.5	166.8	-4.3	-82.0
12	-0.7	62.9	-88.0	94.2	-62.6	52.8	-0.8	160.2
13	-0.8	45.8	-75.4	153.1	-52.5	-2.7	-0.7	130.9
14	-0.9	25.6	-78.8	143.2	-59.8	143.5	-0.2	117.4
15	-1.0	2.1	-64.0	-175.7	-58.7	-9.8	-0.2	104.2
16	-1.2	-25.4	-62.9	141.4	-68.2	97.2	-0.2	92.2
17	-1.4	-55.7	-58.7	121.1	-59.6	145.2	-0.2	79.6
18	-1.5	-88.2	-56.8	76.6	-50.4	-101.6	-0.3	67.6
19	-1.6	-122.3	-64.9	33.6	-35.9	-155.0	-0.2	54.3
20	-1.7	-155.1	-59.8	31.9	-22.8	130.0	-0.5	38.7
21	-1.7	173.5	-61.7	12.5	-17.2	40.2	-0.8	22.1
22	-1.6	144.7	-61.8	-20.2	-13.4	-19.7	-1.2	2.7
23	-1.7	116.7	-67.9	-61.4	-7.9	-69.3	-2.3	-22.5
24	-1.9	89.2	-70.4	-103.5	-0.9	-124.0	-4.8	-56.1
25	-2.2	61.8	-53.6	-7.3	6.9	173.3	-11.6	-100.8
26	-2.6	29.3	-55.3	26.4	15.6	97.3	-17.3	86.7
27	-4.9	-10.7	-58.9	-86.2	24.1	-16.5	-9.6	24.7
28	-7.5	-27.5	-60.7	2.2	24.4	-135.8	-8.0	-4.0
29	-8.6	-59.1	-54.8	-15.2	23.8	132.2	-7.1	-43.7
30	-13.6	-100.9	-48.3	-59.0	23.8	42.5	-10.6	-81.8
31	-28.1	-84.5	-47.7	-87.7	23.8	-47.5	-14.7	-98.0
32	-17.0	-9.0	-47.0	-151.8	25.0	-147.9	-10.9	-157.0
33	-10.0	-50.1	-54.1	-173.9	21.8	85.7	-7.2	110.0
34	-7.4	-81.2	-57.0	95.0	13.8	-20.1	-5.6	58.0
35	-6.1	-109.3	-54.1	107.8	4.5	-104.1	-3.8	29.4
36	-5.1	-140.7	-51.0	61.4	-4.0	-175.3	-2.6	4.4
37	-4.8	-171.4	-52.5	-95.5	-12.0	120.0	-1.8	-13.6
38	-5.8	149.6	-57.9	25.7	-19.4	55.8	-1.2	-35.0
39	-14.6	71.5	-53.2	148.8	-26.4	-23.9	-1.1	-49.4
40	-6.2	-133.6	-53.3	-158.0	-41.9	-98.5	-0.9	-61.8

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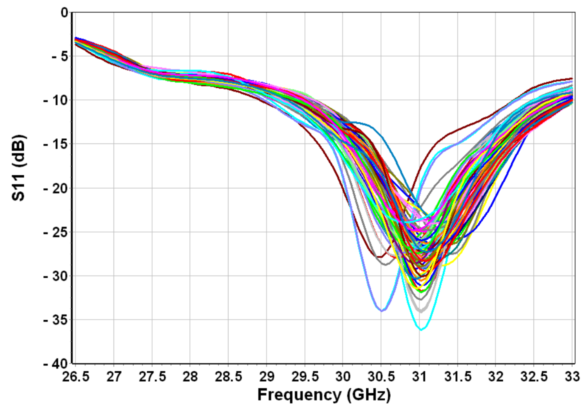
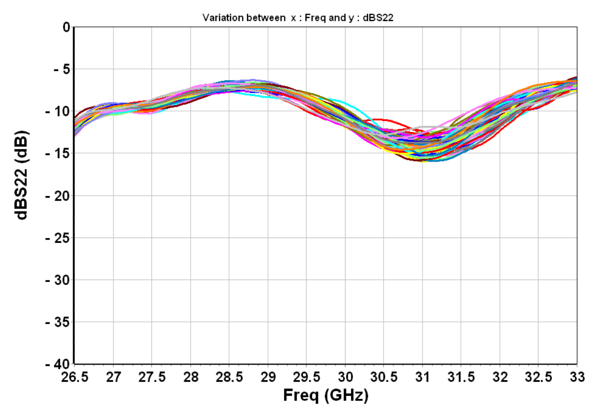
Typical On Wafer Measurements : Small signal Performances

Test conditions: Tcase=+25°C, Vd = +20V, Id = 280mA, 82 Chips, Pulsed Signal (25µs, 10%)

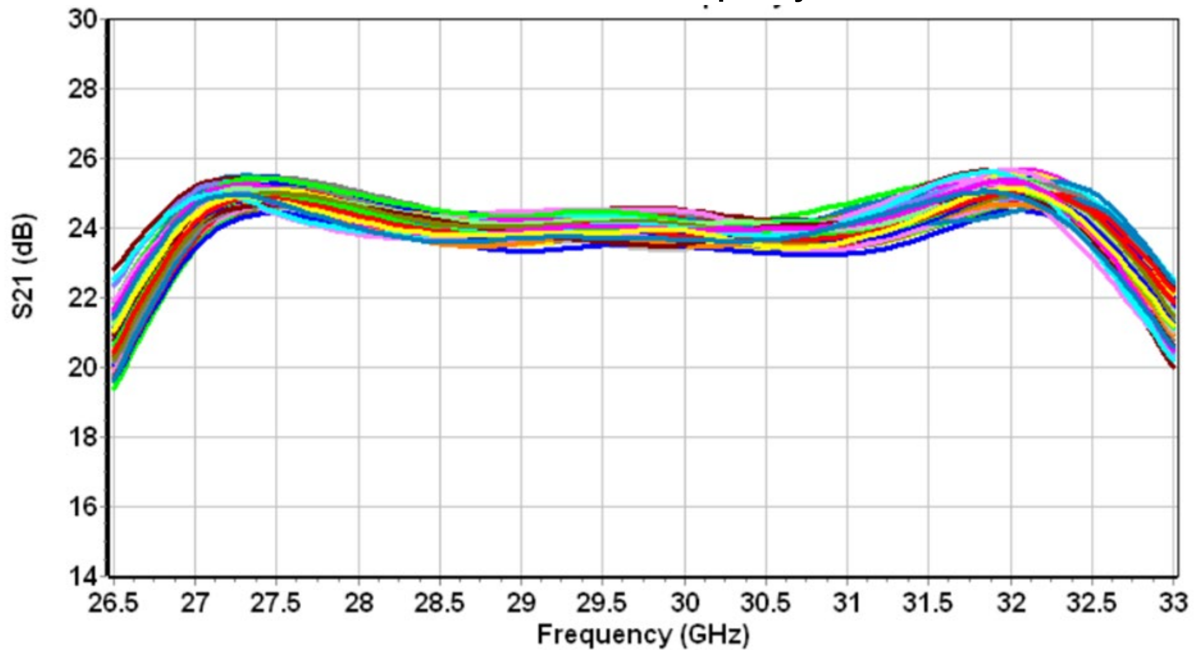
Input Return Losses versus Frequency



Output Return Losses versus Frequency



Linear Gain versus Frequency



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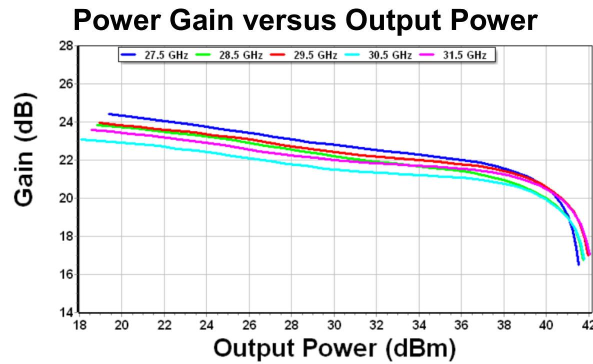
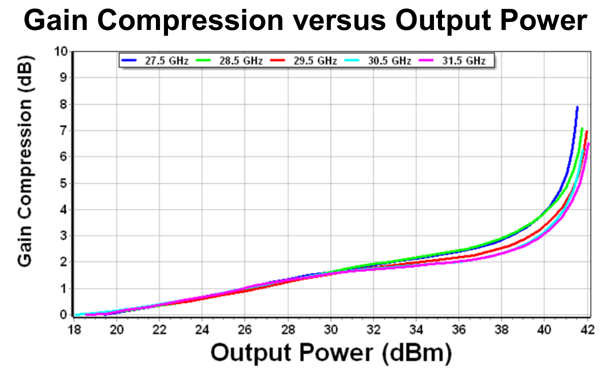
Typical On Wafer Measurements : Large Signal Performances

Test conditions : Tcase=+25°C, Vd = +20V, Id = 280mA, 1 Chip, Pulsed Signal (25µs, 10%)

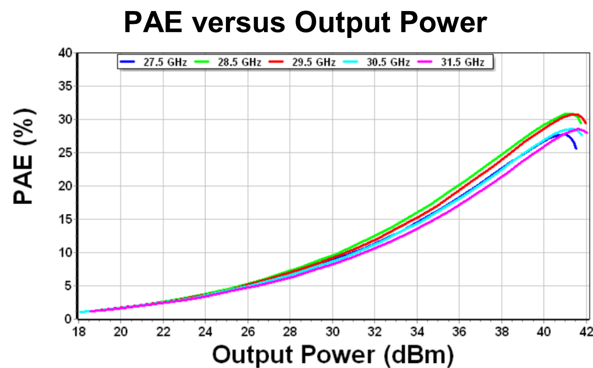
Power Gain versus Output Power



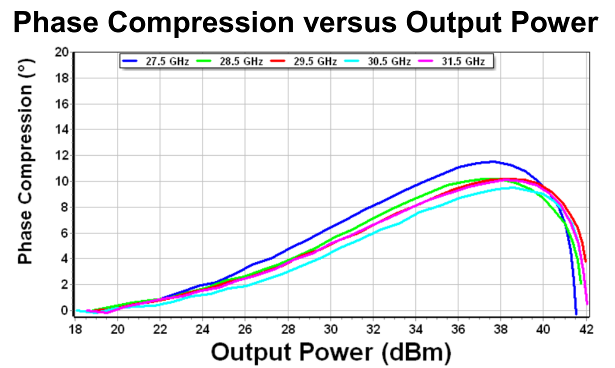
Gain Compression versus Output Power



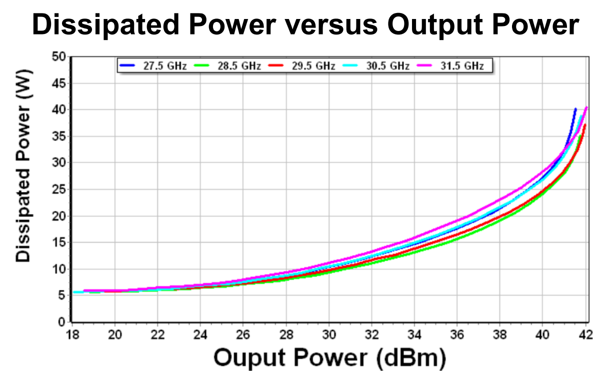
PAE versus Output Power



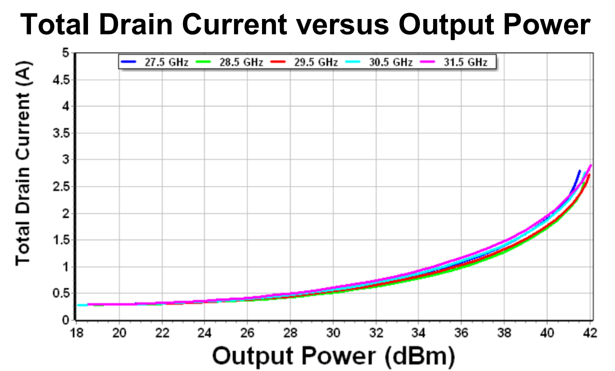
Phase Compression versus Output Power



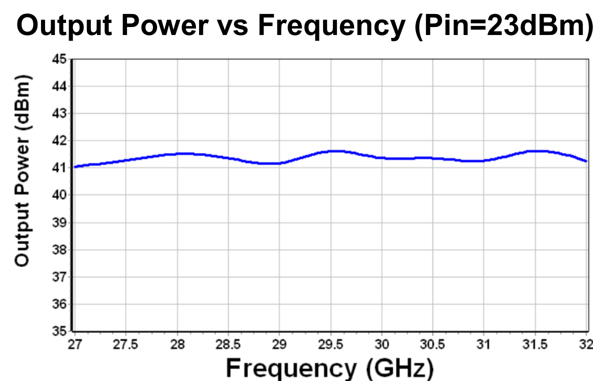
Dissipated Power versus Output Power



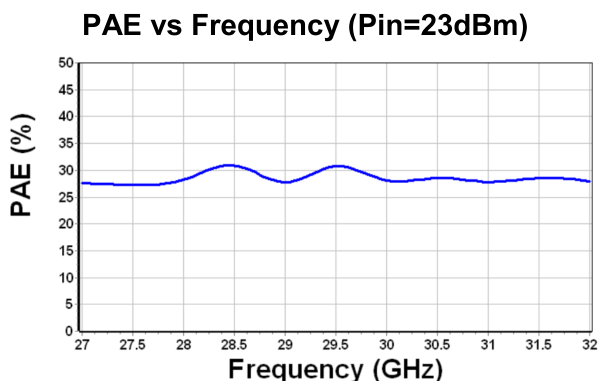
Total Drain Current versus Output Power



Output Power vs Frequency (Pin=23dBm)



PAE vs Frequency (Pin=23dBm)



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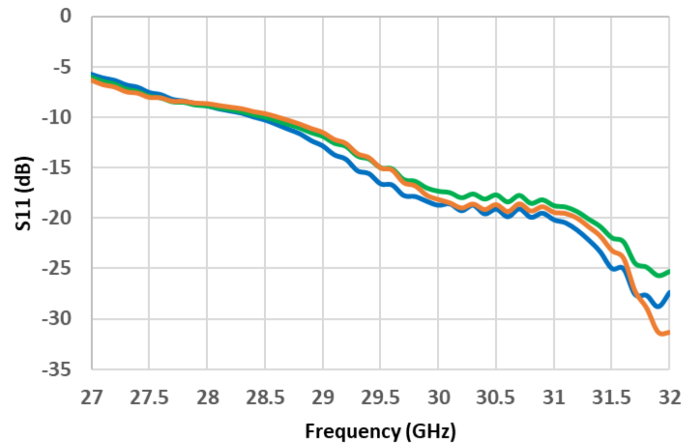
Typical Board Measurements : Small Signal Performances

Measurement reference plane is de-embedded at the wire bondings plane on the RF feed line.

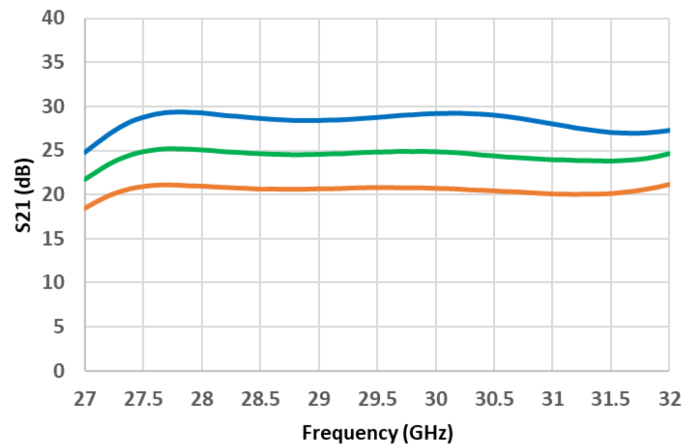
Performances versus temperature

Test conditions : Tcase= -40°C / +25°C / +85°C, Vd = +20V, Id = 280mA

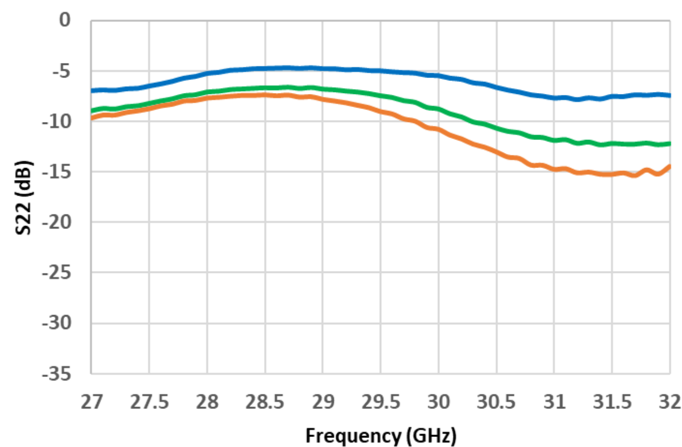
Input Return Losses versus Frequency and Temperature



Linear Gain versus Frequency and Temperature



Output Return Losses versus Frequency and Temperature



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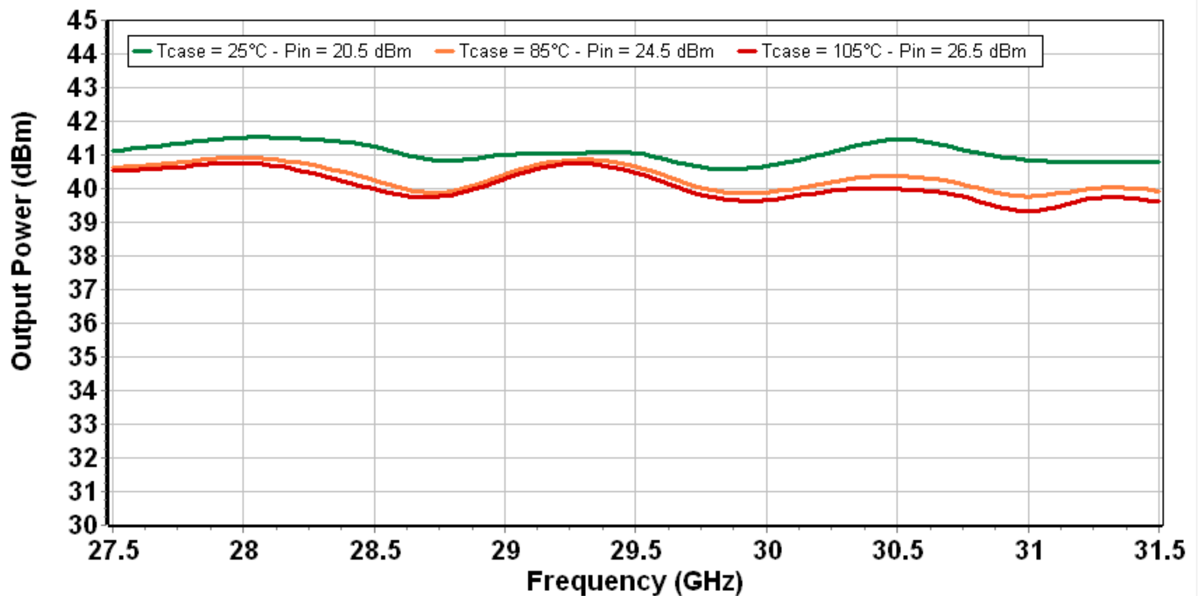
Typical Board Measurements : Large Signal Performances

Measurement reference plane is de-embedded at the wire bondings plane on the RF feed line.

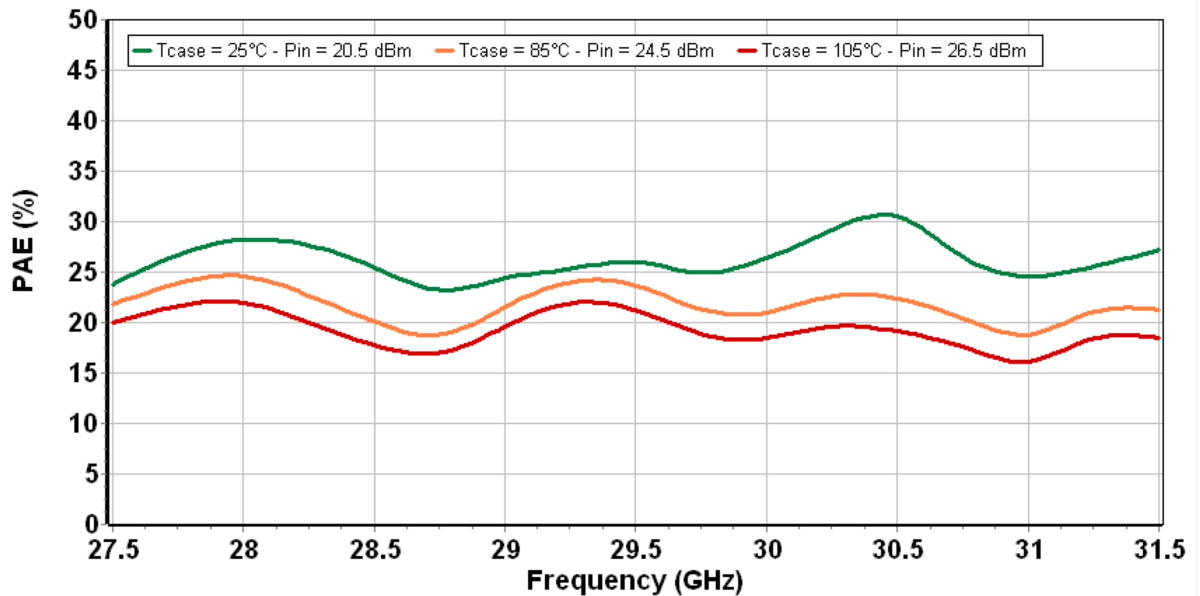
Performances versus Frequency and Temperature

Test conditions : Tcase= +25°C / +85°C / +105°C, Vd = +20V, Id = 280mA, CW signal

Output Power versus Frequency and Temperature



Power Added Efficiency versus Frequency and Temperature



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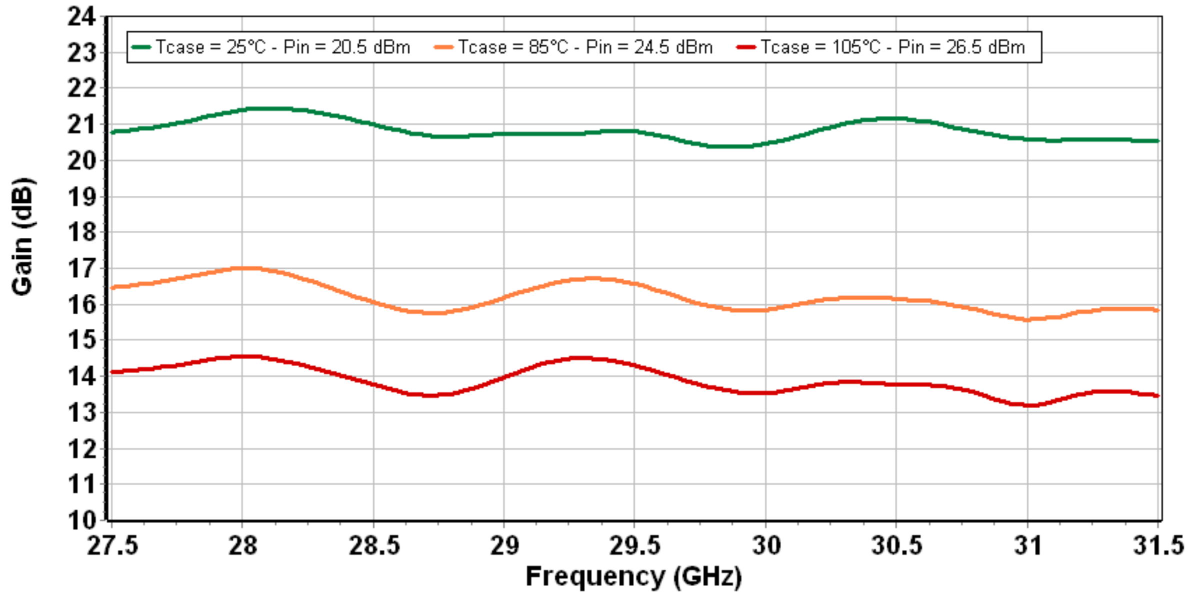
Typical Board Measurements : Large Signal Performances

Measurement reference plane is de-embedded at the wire bondings plane on the RF feed line.

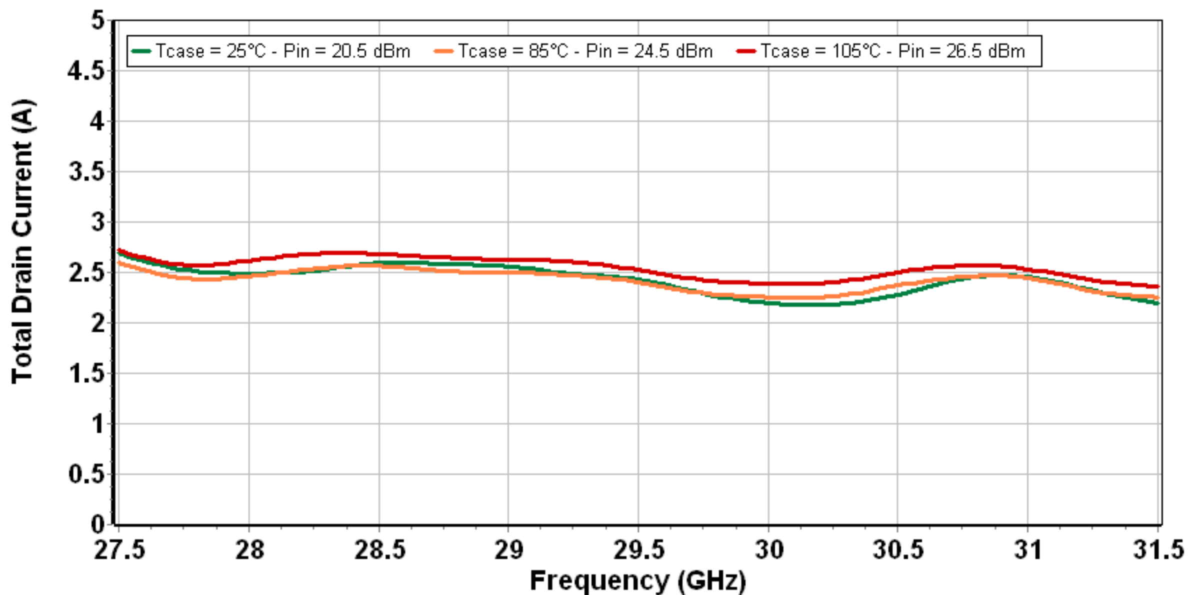
Performances versus Frequency and Temperature

Test conditions : Tcase= +25°C / +85°C / +105°C, Vd = +20V, Id = 280mA, CW signal

Gain versus Frequency and Temperature



Drain Current versus Frequency and Temperature



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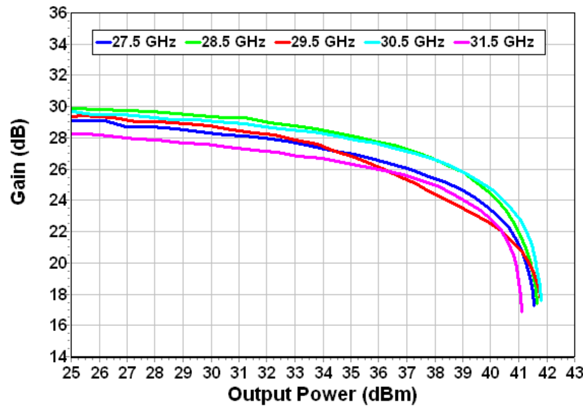
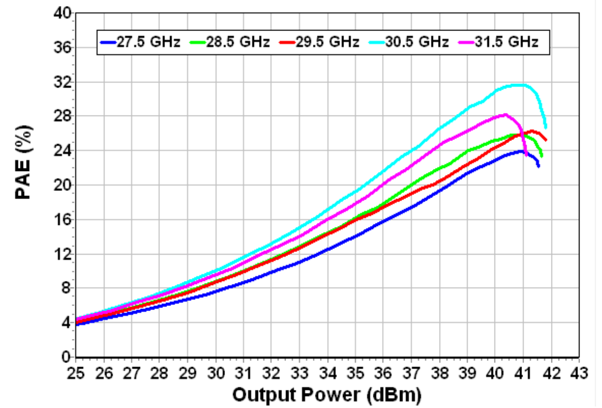
Typical Board Measurements : Large Signal Performances

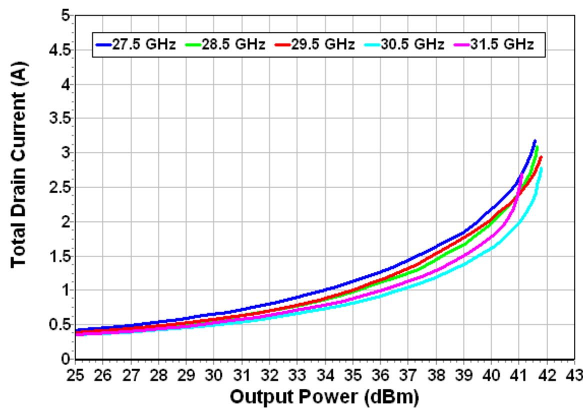
Measurement reference plane is de-embedded at the wire bondings plane on the RF feed line.

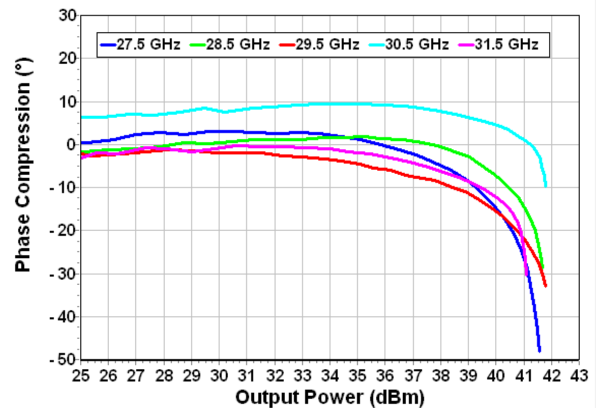
Performances versus output power and frequency

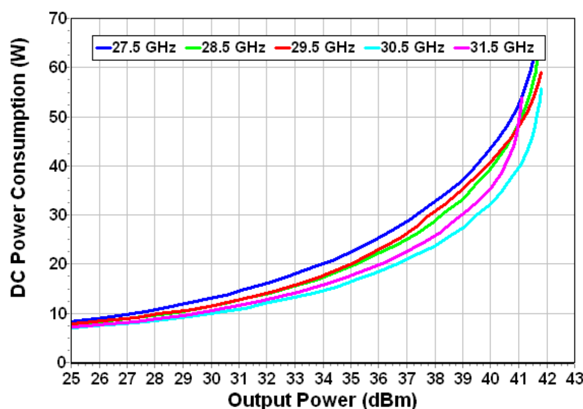
Test conditions : Tcase= +25°C, Vd = +20V, Id = 280mA, CW signal

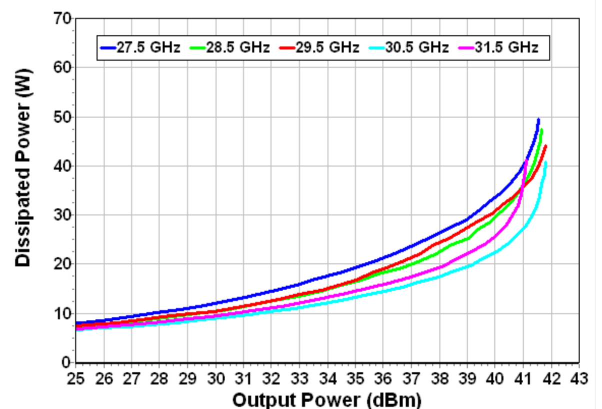












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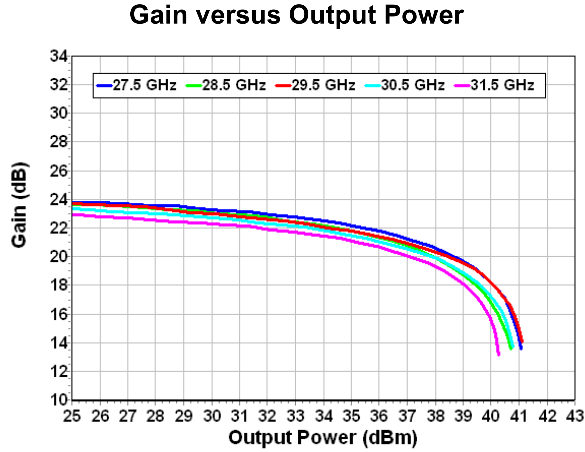
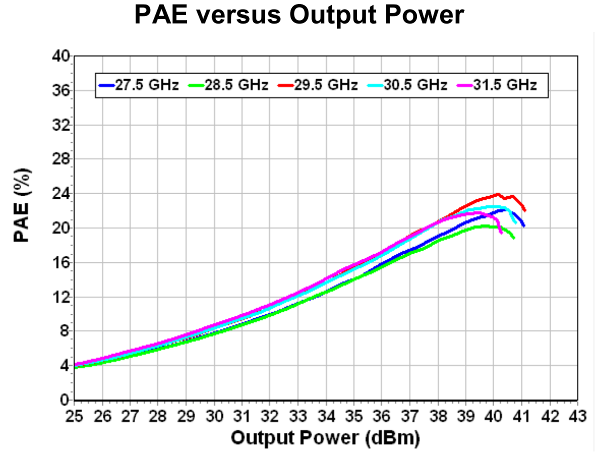
Typical Board Measurements : Large Signal Performances

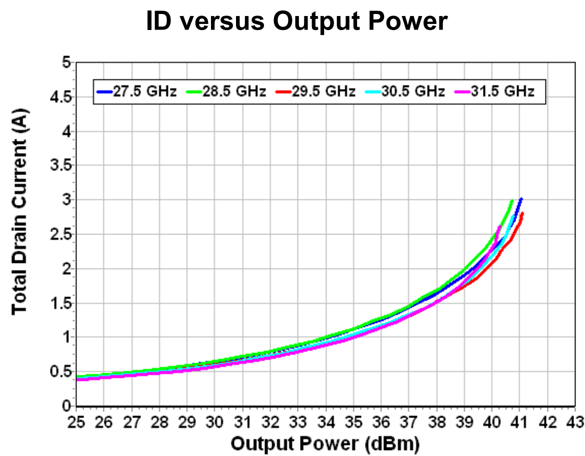
Measurement reference plane is de-embedded at the wire bondings plane on the RF feed line.

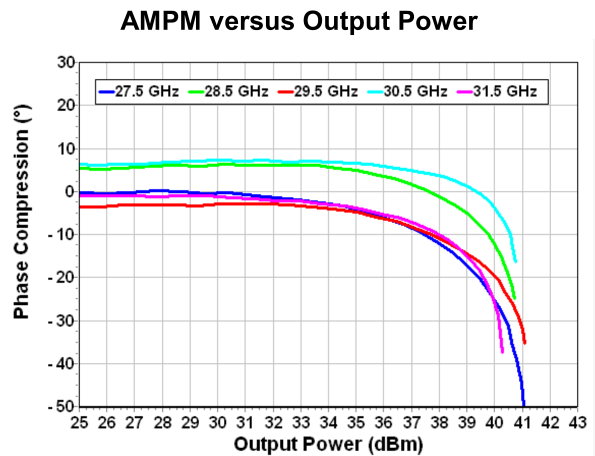
Performances versus output power and frequency

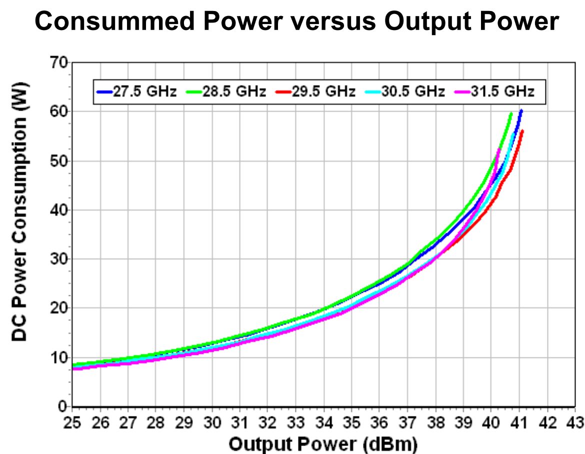
Test conditions : Tcase= +85°C, Vd = +20V, Id = 280mA, CW signal

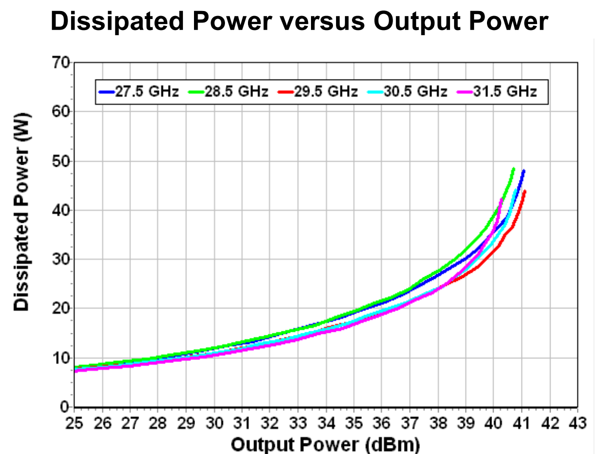












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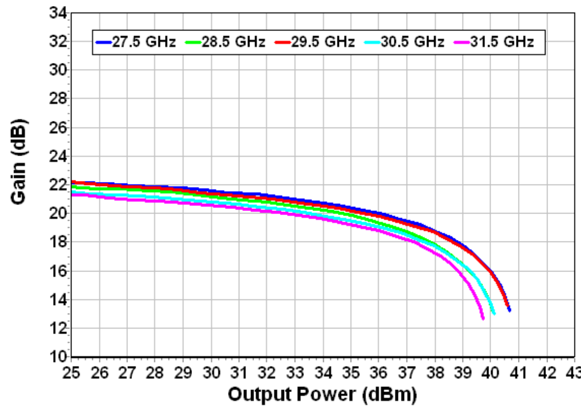
Typical Board Measurements : Large Signal Performances

Measurement reference plane is de-embedded at the wire bondings plane on the RF feed line.

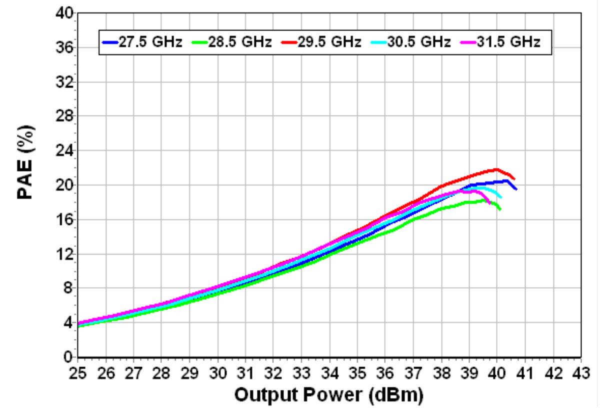
Performances versus output power and frequency

Test conditions : Tcase= +105°C, Vd = +20V, Id = 280mA, CW signal

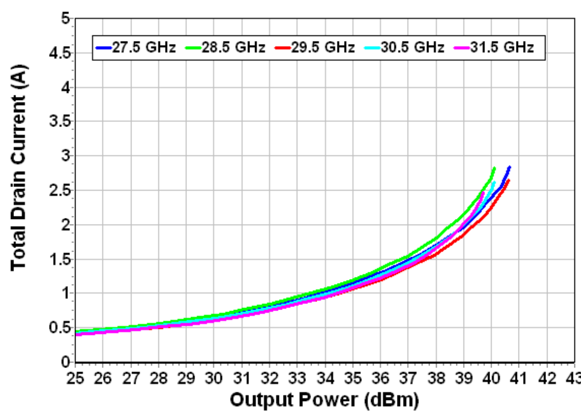
Gain versus Output Power



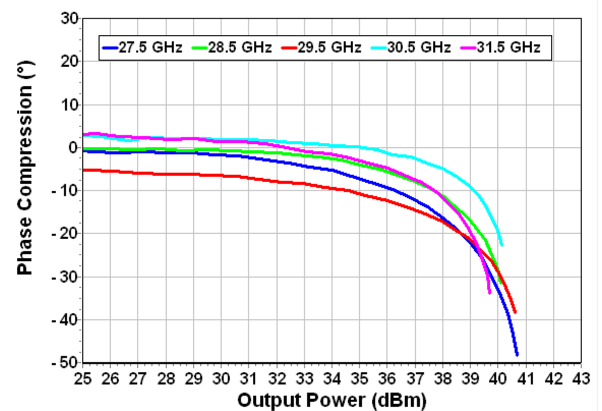
PAE versus Output Power



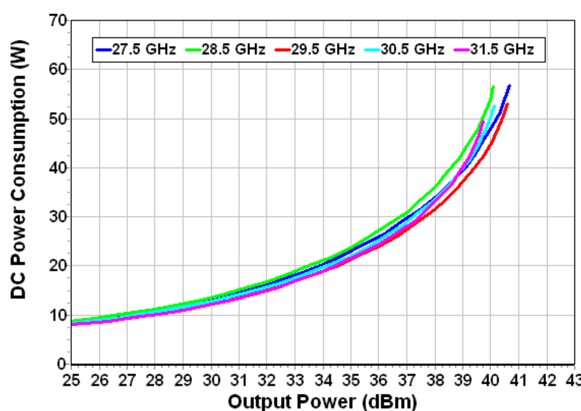
ID versus Output Power



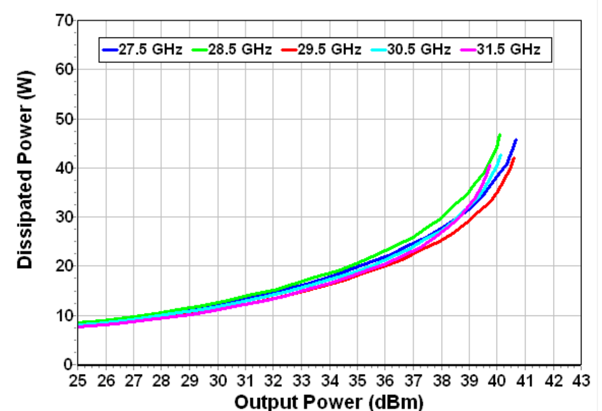
AMPM versus Output Power



Consummed Power versus Output Power



Dissipated Power versus Output Power



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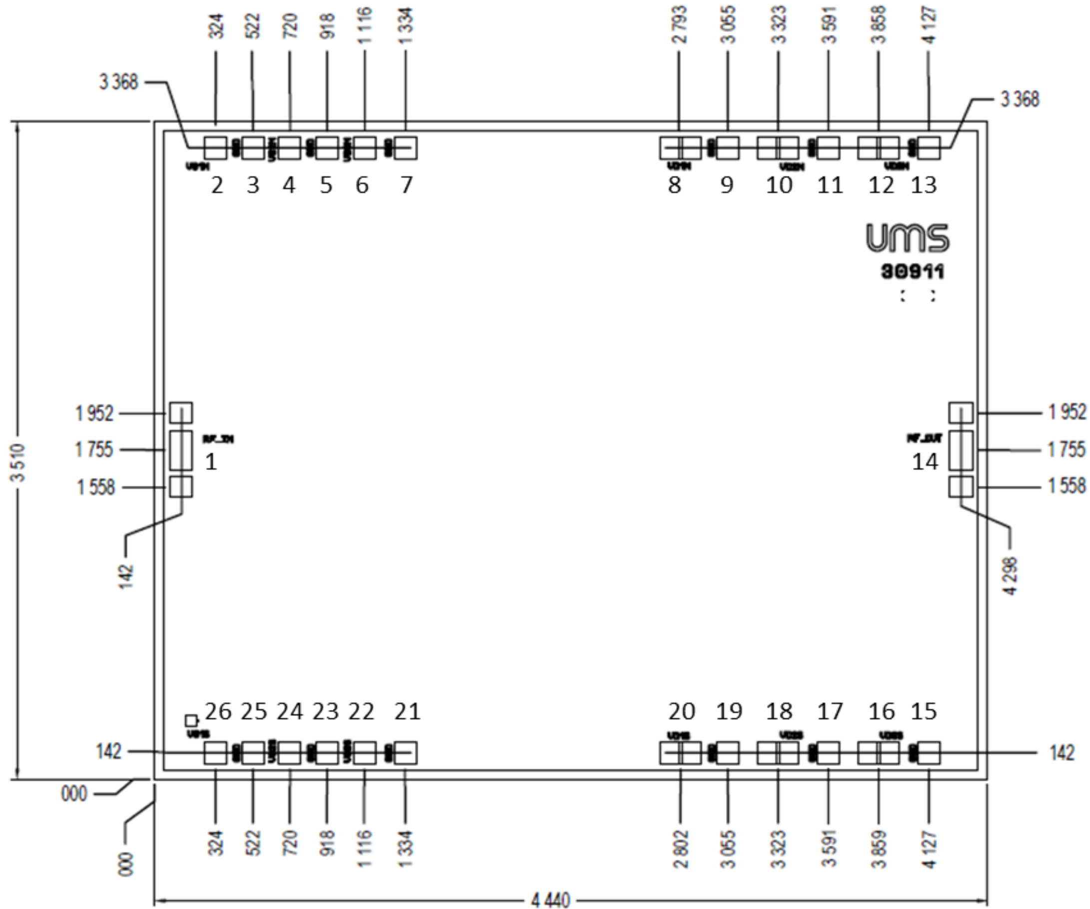
Chip Mechanical Data



All dimensions are in micrometres
The size is 4440±50 x 3510±50 µm²
The chip thickness is 70±10 µm

DC pads (2, 3, 4, 5, 6, 7, 9, 11, 13, 15, 17, 19, 21, 22, 23, 24, 25, 26) size is 116x116 µm²
DC pads (8,10, 12, 16, 18, 20) opening is 216x116 µm²
DC pads (1, 14) opening is 206x116 µm²

1-	RF_IN	10-	VD2N	19-	GND
2-	VG1N	11-	GND	20-	VD1S
3-	GND	12-	VD3N	21-	GND
4-	VG2N	13-	GND	22-	VG3S
5-	GND	14-	RF_OUT	23-	GND
6-	VG3N	15-	GND	24-	VG2S
7-	GND	16-	VD3S	25-	GND
8-	VD1N	17-	GND	26-	VG1S
9-	GND	18-	VD2S		

(1) Ground all pins marked “GND” through the PCB board is strongly recommended. Ensure that the PCB board is designed to provide the best possible ground to the package.

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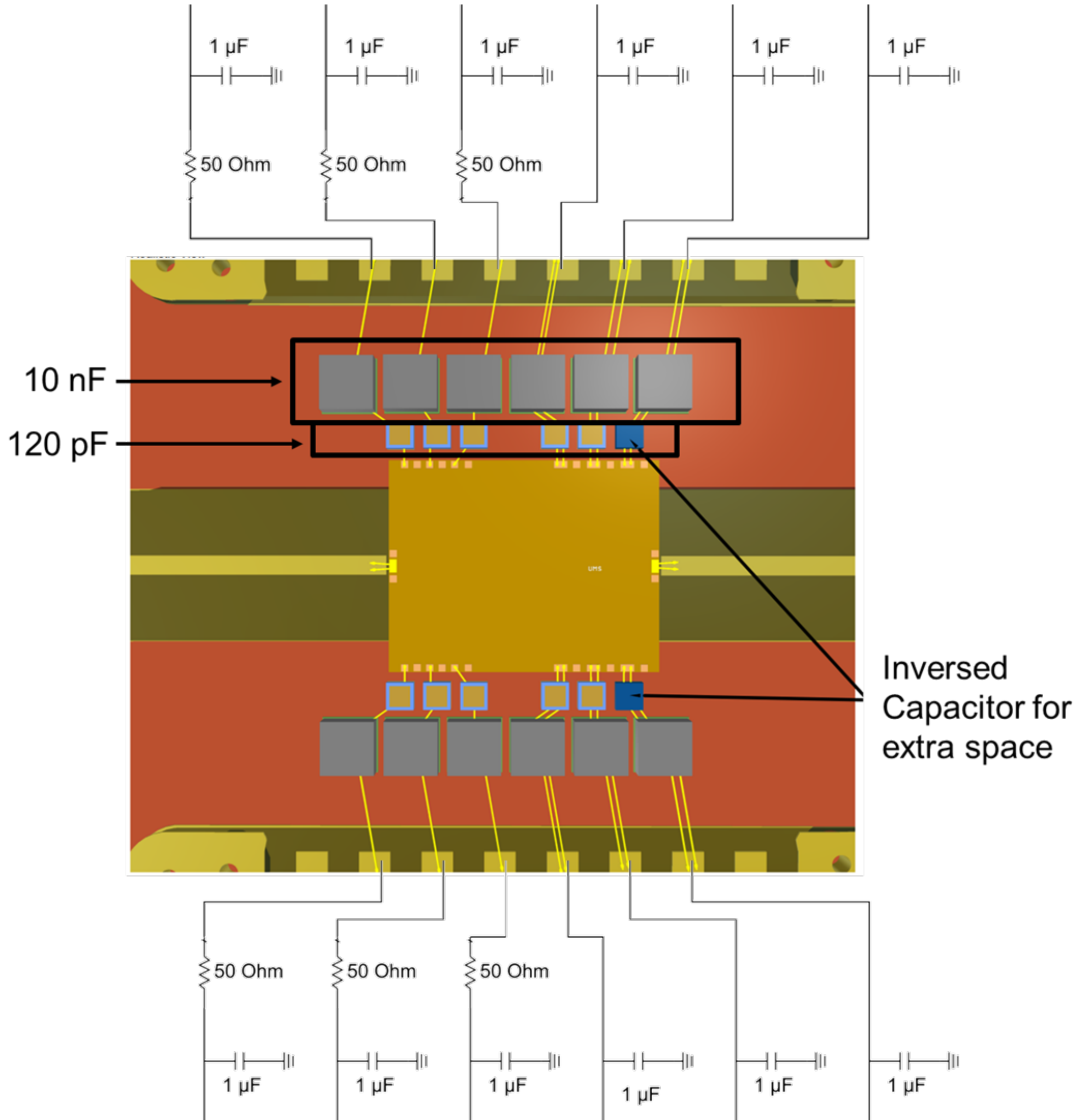
Recommended assembly plan



The decoupling network used is composed of 3 levels of parallel capacitors. The first level is 120pF chip capacitor, the second level is 10nF chip capacitor and the third level is 1µF SMD 1210 capacitor. The two firsts levels should be as close as possible of to the die. A 50Ω serie resistor was added on each gate supply.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
VD1N, VD1S, VD2N, VD2S, VD3N, VD3S	Vd	120pF 10nF 1µF	Drain Supply
VG1N, VG1S, VG2N, VG2S, VG3N, VG3S	Vg	120pF 10nF 50Ω 1µF	Gate Supply

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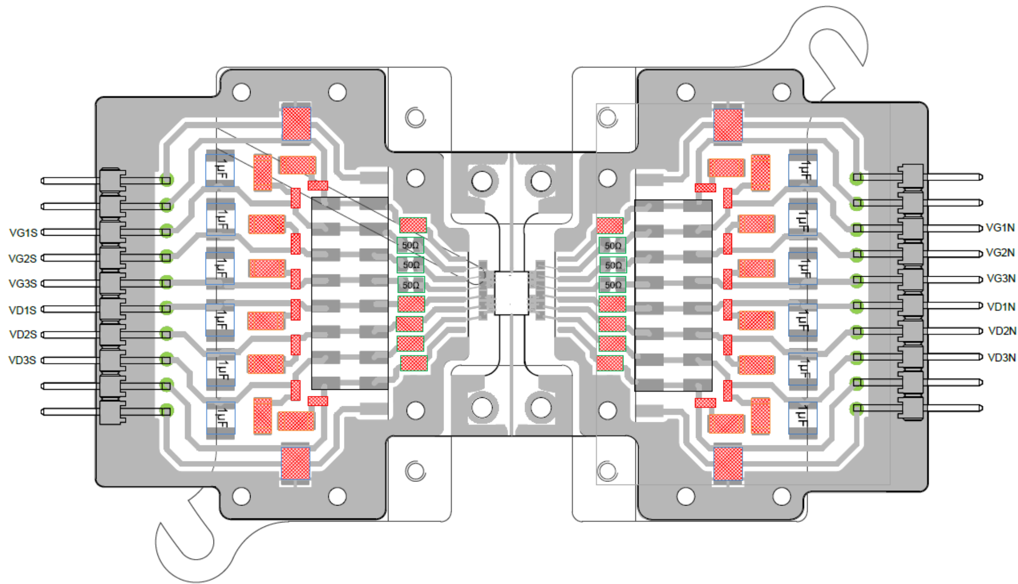
Evaluation mother board



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

ESD sensitivity

Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)
ESD STM5.1-1998	HBM Class 0 (<250V)

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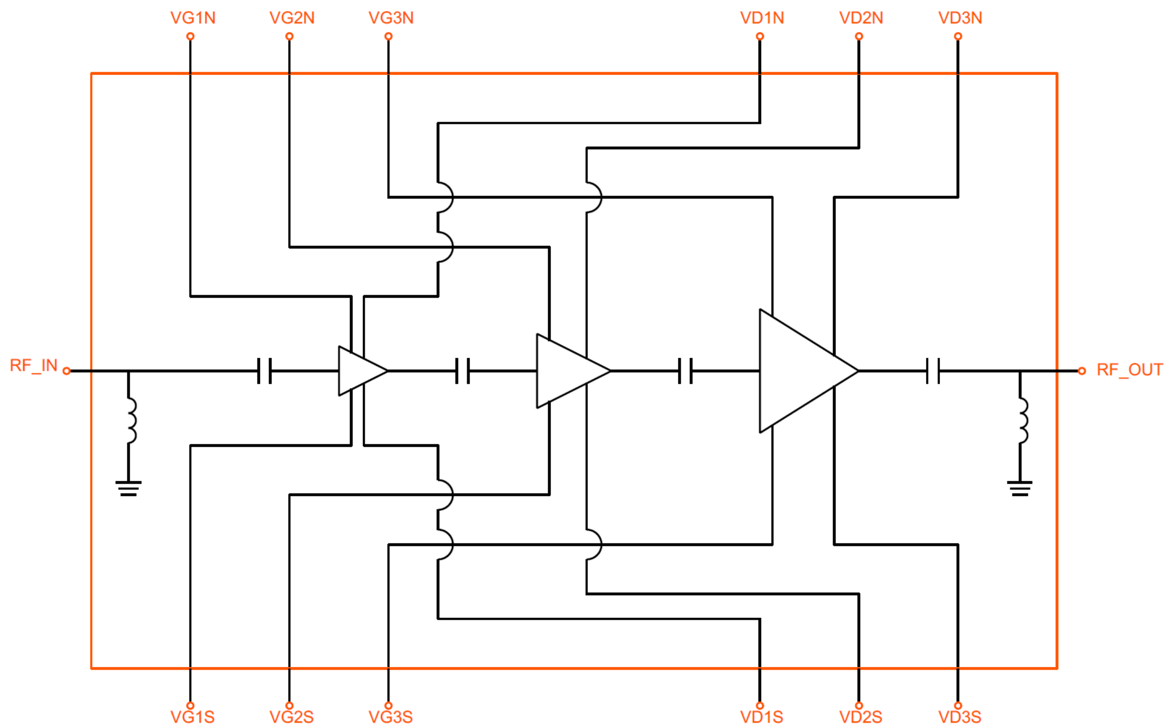
DC Schematic



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Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Chip form : CHA8262-99F/00

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