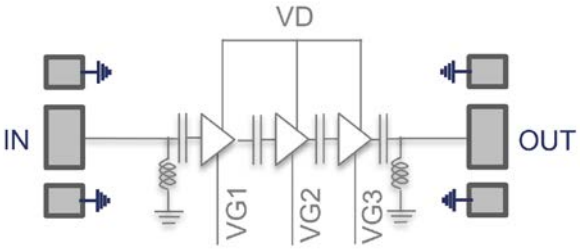
CHA2595-98F

27.5-43.5GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in bare die

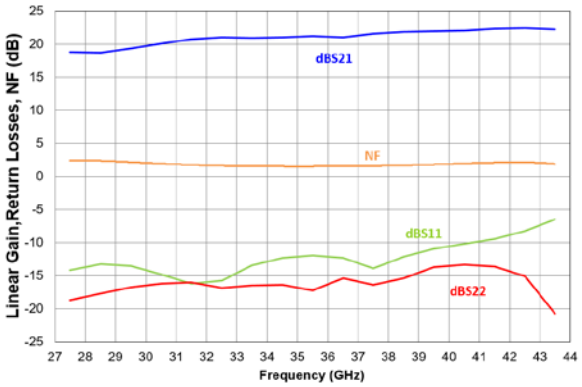
Description

This circuit is a wide band monolithic Low Noise Amplifier with state of the art wide band, low noise and adjustable gain performance.
It is designed for a wide range of applications, from military to commercial communication and test instrumentation systems.
It is manufactured with a successfully space evaluated pHEMT process, 100nm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
ESD protection on DC/RF is included in the product.



Main Features

- Broadband performances: 27.5-43.5GHz
- Typical Linear Gain:19.5dB
- Typical Noise Figure: 2dB
- P_{1dB}: 11dBm
- P_{sat}: 12dBm
- OIP3: >20dBm
- DC bias: Vd=3.3V@Id=61mA
- Size : 2350 x 1150 µm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.5		43.5	GHz
Gain	Linear Gain	18	19.5		dB
NF	Noise Figure		2	2.4	dB
P_{1dB}	Output Power @1dB gain comp.	8	11	13.5	dBm

United Monolithic Semiconductors S.A.S.
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Electrical Characteristics

Tamb.= +25°C, Vd (D) = 3.3V, Vg (G1=G2=G3) set in order to get Idq = 61mA (≈0V)

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	27.5		43.5	GHz
Gain	Linear Gain 27.5 GHz 29GHz 32 GHz 38 GHz 42 GHz 43.5 GHz		 19 19.5 21 21.0 21.5 22		dB
NF	Noise Figure 27.5 GHz 29GHz 32 GHz 38 GHz 42 GHz 43.5 GHz		 2.5 2.2 1.7 1.4 2.1 1.9		dB
IRL	Input return loss		10		dB
ORL	Output return loss		10		dB
P_{1dB}	Output power at 1dB gain comp 27.5 GHz 29-32 GHz 33-38 GHz 39-43 GHz		 8.0 >9.5 >11 >12		dBm
P_{sat}	Output power at 3dB gain comp 27.5GHz 29-32 GHz 33-38 GHz 39-43 GHz		 9.0 >10.5 >11.5 >13.5		dBm
OIP3	Output 3rd order intercept point		20		dBm
Vd	Drain bias voltage	3.0	3.3	3.5	V
Id	Drain bias current		61		mA

These values are representative of on-wafer measurements as defined on the drawing in paragraph "Evaluation mother board".

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.0	V
Vg	Gate bias voltage	-1.5 to +0.4	V
Pin	RF input power	-4	dBm
Tj	Maximum Junction temperature (2)	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Thermal Resistance channel to ground paddle (see “Device thermal performances” in the following)

Recommended Operating Range 3, 4

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	3.0 to 3.6	V
Idq	Drain bias current	60 to 90	mA
Vg	Gate bias voltage	-0.5 to 0.2	V
Pin	Input power range	-20 to -5	dBm

(3) Electrical performances are defined for specified test conditions

(4) Electrical performances are not guaranteed over all recommended operating conditions

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Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Biasing	Parameter	Values	Unit
D	D	DC Drain voltage all stages	3.3	V
G* (1)	G1/G2/G3	DC Gate voltage all stages	≈0	V

(1) Can be adjusted to set Id = 61mA.

“Power ON” sequence

1. Ground the device
2. Bias circuit gate voltage at Vg low enough (Typically Vg ≈ -1V)
3. Apply Vds bias Voltage (Typically Vd to 3.3V)
4. Increase slowly Vgs up to quiescent bias drain current Idq
5. Apply RF signal

“Power OFF” sequence

1. Turn RF power supply off
2. Bias circuit gate voltage at Vg low enough (Typically Vg ≈ -1V)
3. Turn Vds Bias voltage to 0V
4. Set Vg to -1V in order to get Idq = 0mA
5. Set Vg to 0V

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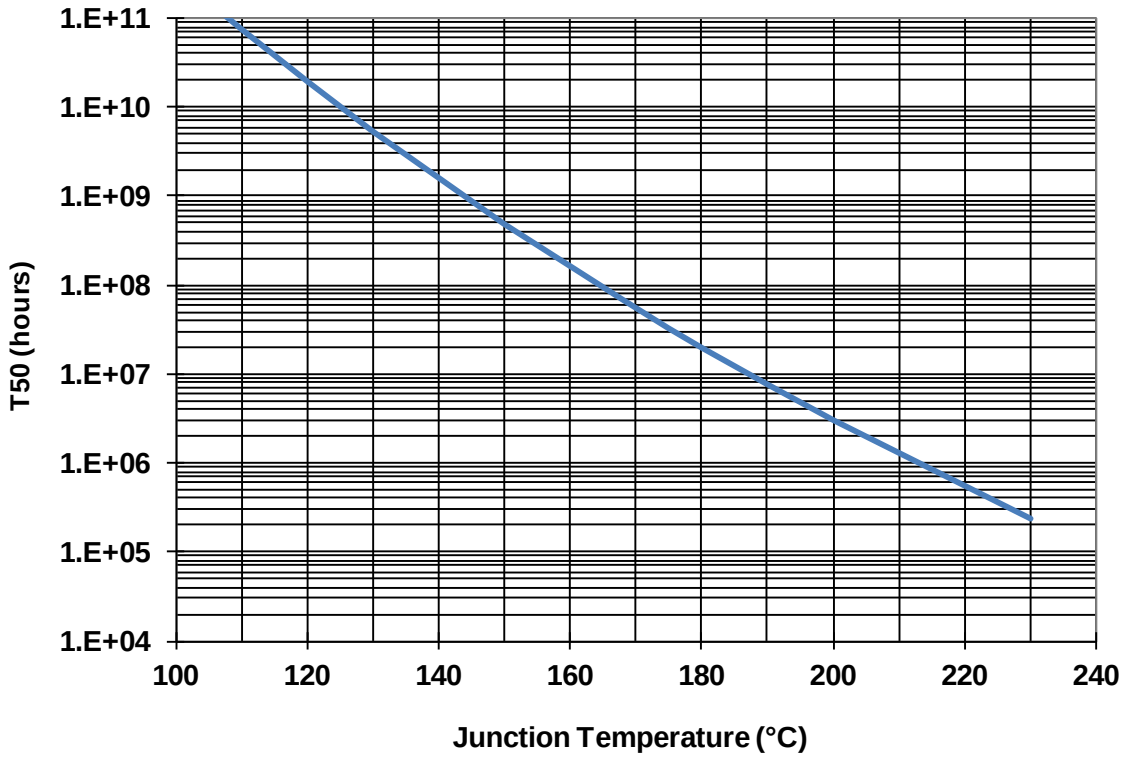
Device thermal performances

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
The temperature Tb_{chip} is defined as the chip backside temperature.
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
Therefore, the PCB system must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd = 3.3V Id = 61mA P_{diss} = 0.2W	101	79	$3.6e^{11}$

(1) Assuming 85°Tb_{chip}



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Typical Sij parameters

Tamb.= +25°C, Vd = +3.3V, Id =61mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
27.5	-14.20	144.69	-45.62	-27.67	18.78	-78.82	-18.70	82.92
28.5	-13.29	91.47	-46.53	-60.73	18.70	-105.23	-17.71	66.58
29.5	-13.55	61.71	-48.97	-80.40	19.29	-130.73	-16.82	47.02
30.5	-14.82	45.92	-47.90	-93.17	20.10	-158.61	-16.20	22.79
31.5	-16.22	41.33	-47.18	-109.48	20.68	172.17	-16.07	-4.88
32.5	-15.78	47.01	-45.59	-144.46	21.00	142.23	-16.91	-27.05
33.5	-13.46	38.34	-47.61	-173.20	20.89	114.11	-16.46	-44.35
34.5	-12.30	20.38	-47.50	158.74	21.00	88.36	-16.40	-63.85
35.5	-11.96	4.49	-48.41	119.64	21.16	61.14	-17.21	-70.20
36.5	-12.36	-10.72	-56.04	96.76	21.03	35.74	-15.44	-78.32
37.5	-13.92	-11.38	-54.86	-168.02	21.53	10.03	-16.38	-86.82
38.5	-12.13	-9.68	-50.63	135.49	21.78	-18.72	-15.37	-82.81
39.5	-10.99	-17.71	-48.67	97.63	21.89	-46.06	-13.77	-93.46
40.5	-10.25	-24.07	-50.21	68.85	22.04	-74.72	-13.36	-104.92
41.5	-9.49	-27.75	-52.21	45.13	22.28	-104.58	-13.63	-117.91
42.5	-8.25	-29.81	-53.17	48.57	22.38	-136.88	-15.08	-132.00
43.5	-6.55	-34.65	-56.76	-7.46	22.21	-171.58	-20.73	-153.16

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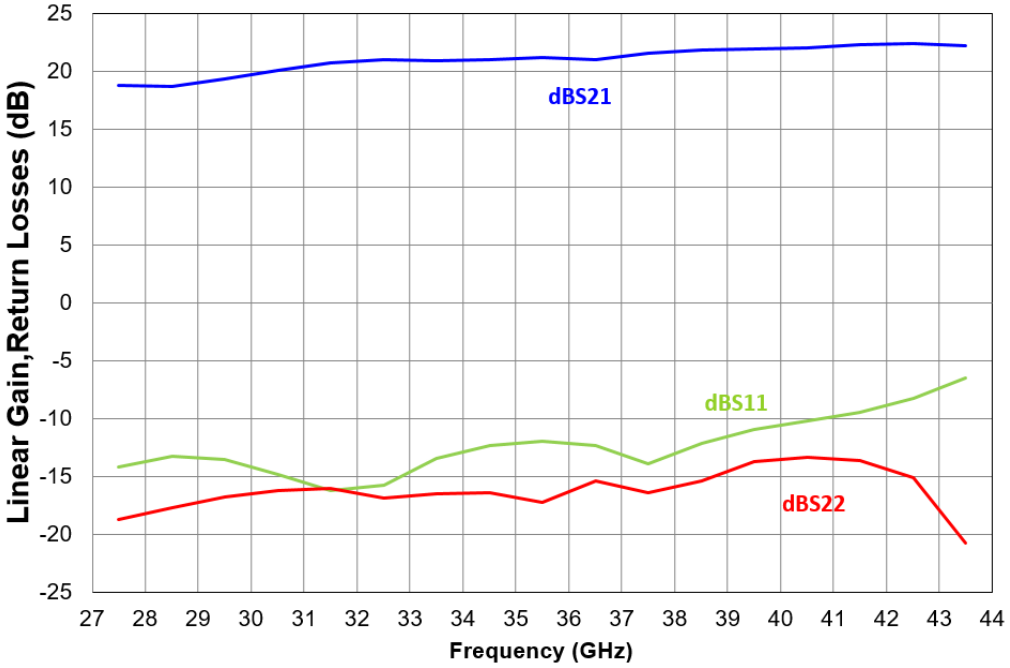
Typical Board S-Parameters Measurements

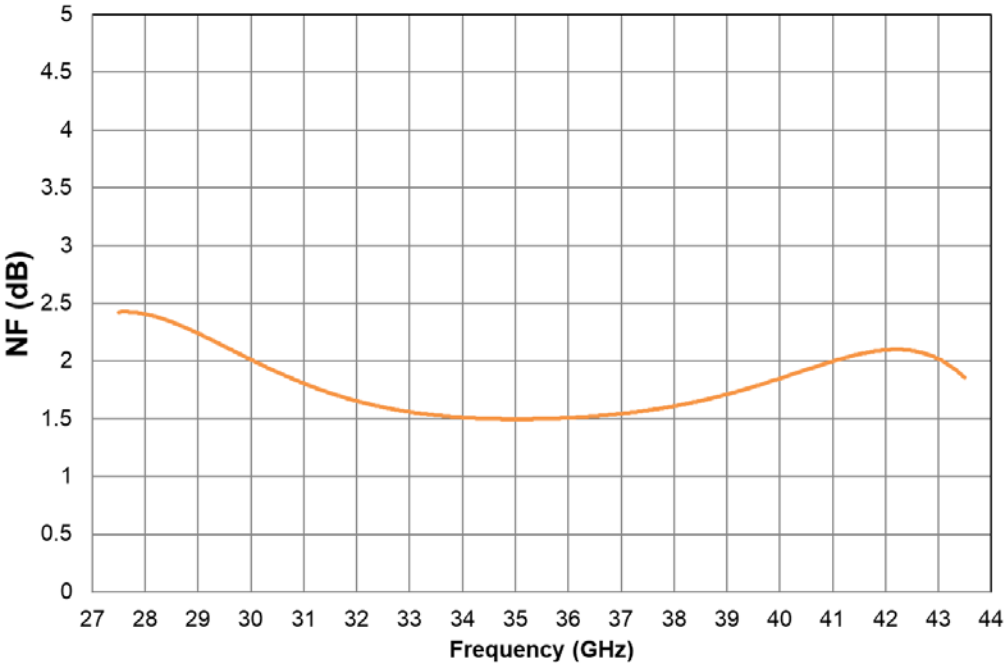
Tamb.= +25°C, Vd = 3.3V

All graphs presented with on-wafer measurement in the access plans of the die.

Linear Gain and Return Losses versus Frequency



Noise Figure with Vd = 3.3V, VG = 0V



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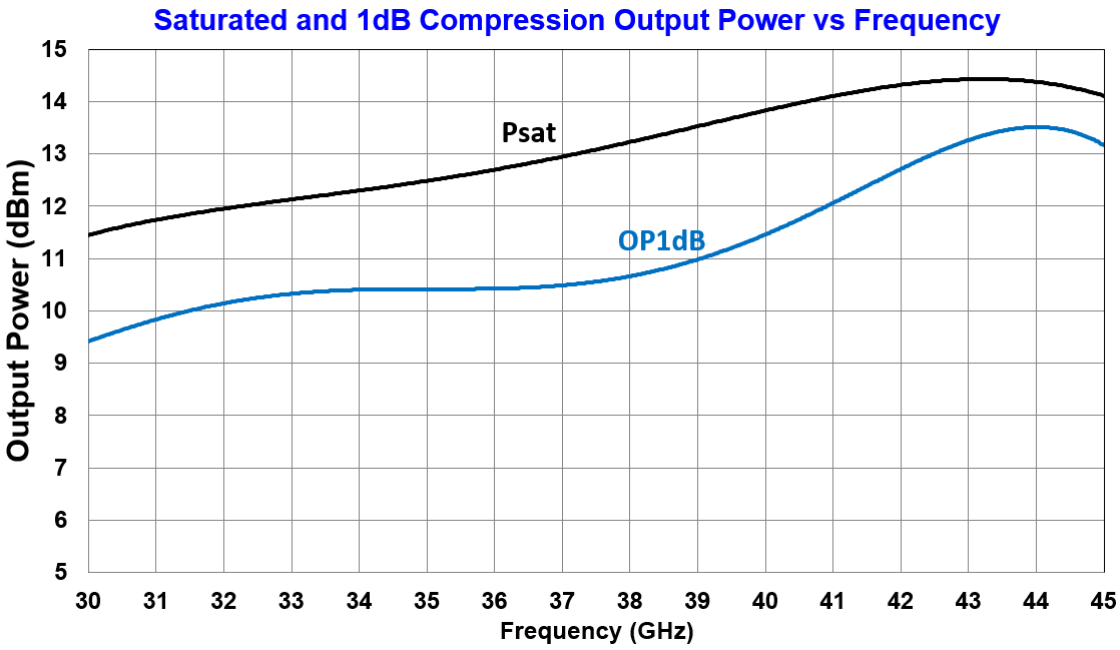
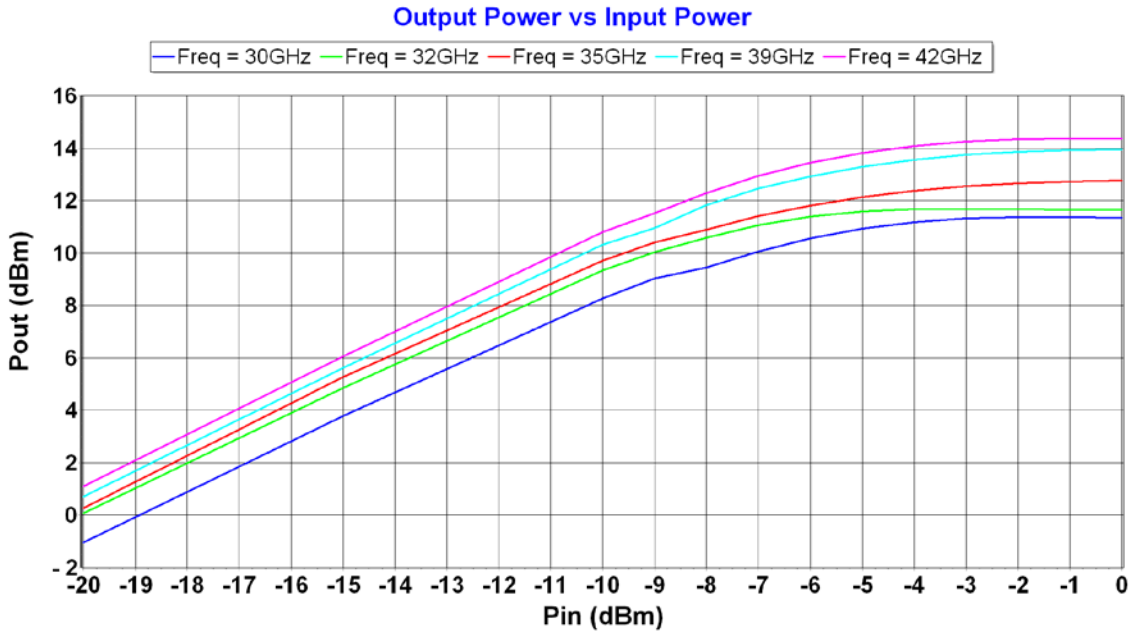
Typical Board Power Measurements

Tamb.= +25°C, Vd = 3.3V, Vg = 0V

All graphs presented with on-wafer measurement in the access plans of the die.





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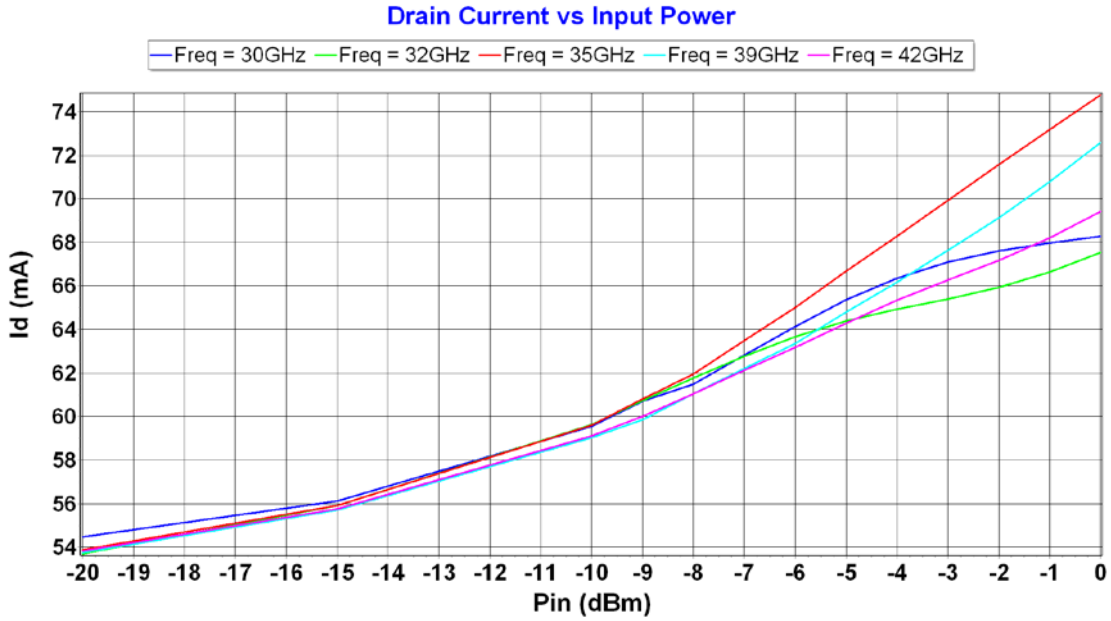

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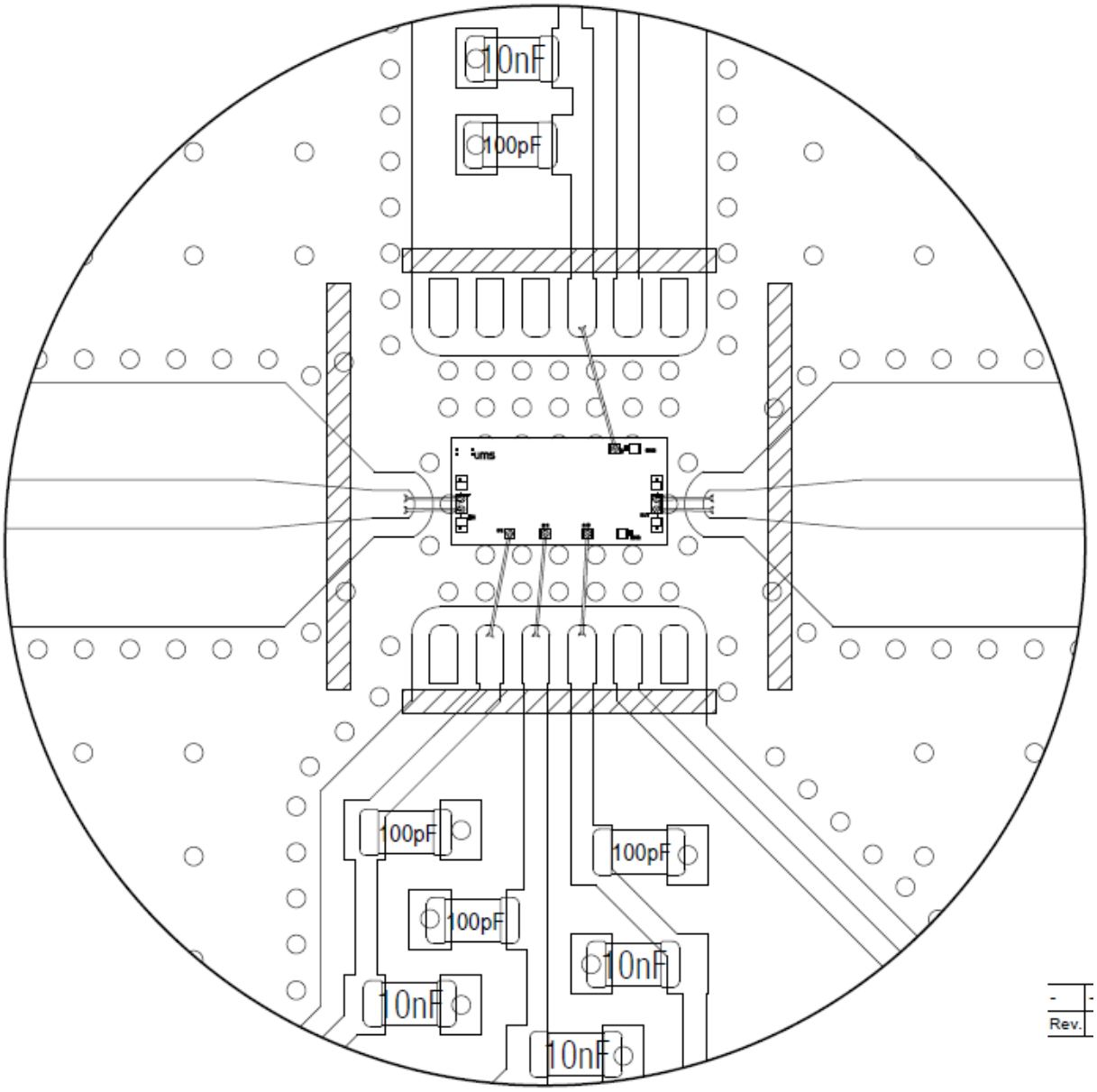
Recommended assembly plan



Decoupling capacitors: 100pF, 10nF (on gate & drain access)

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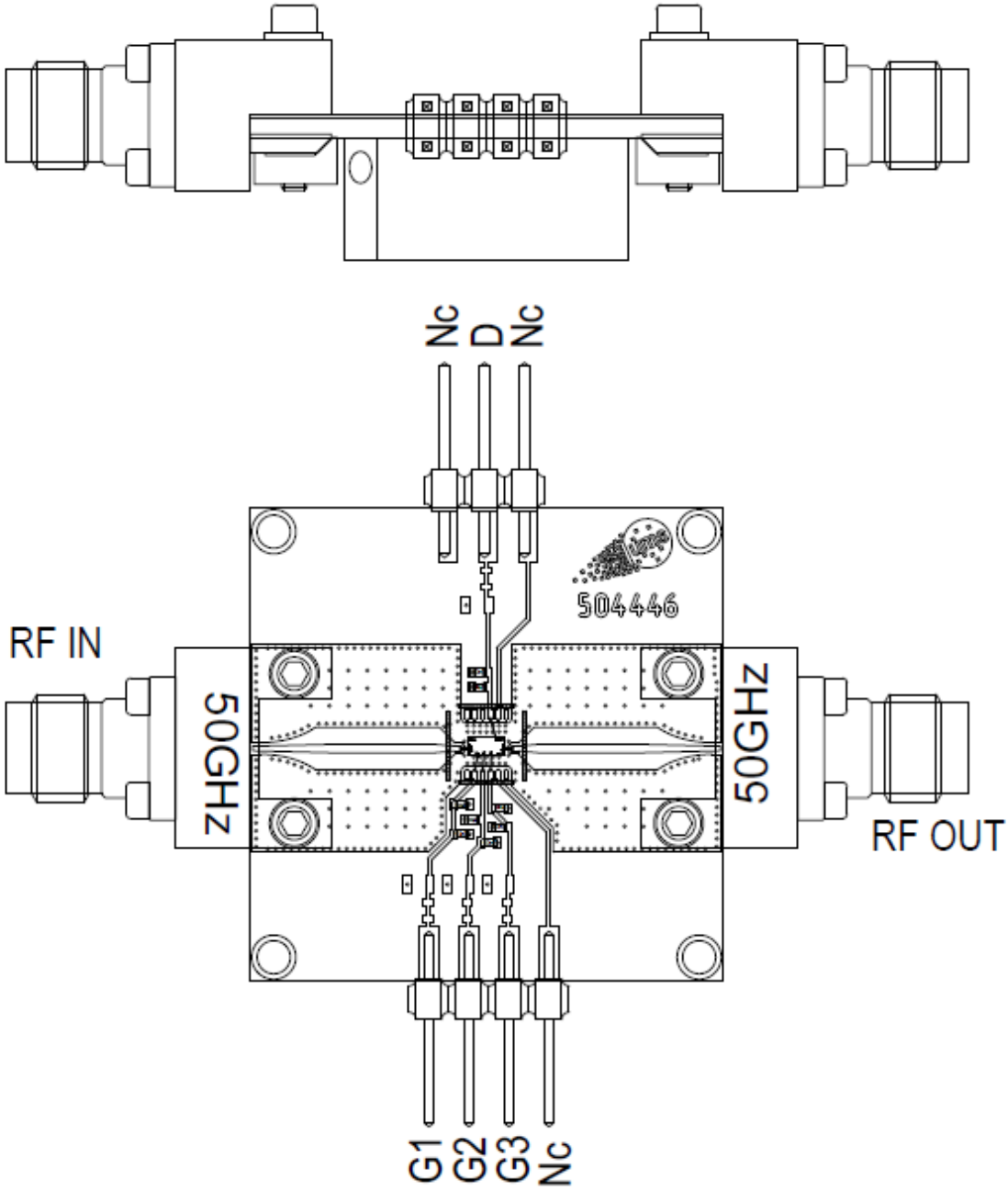
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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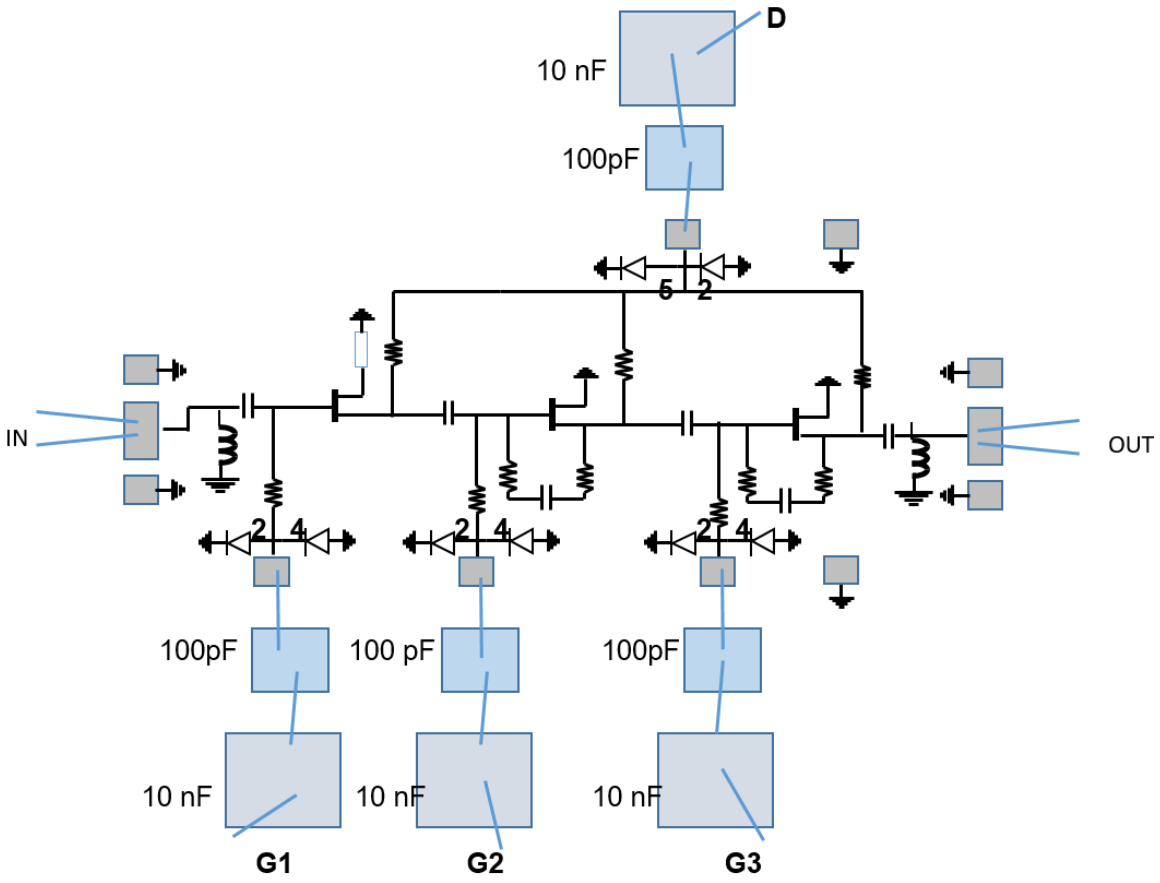
DC Schematic & biasing



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Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

ESD protections are also implemented on gate and drain accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Bare Die:	CHA2595-98F

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