Protec GmbH
High-Rel Electronic Components
SPACE COMPONENTS NEWSLETTER *Mai 2020*

NX NanoXplore

IPs ready to use in NXmap:

Interface:
- APB slave to serial master

Debug:
- Scope
- Startup Scope

Bus:
- SER/DES
- MIL-STD-1553
- AHB2AHB
- AHBCTRL
- AHBUART
- APBCTRL
- APBUART
- GR1553B
- GRCANFD
- GRETH
- GRGPIO
- GRPCI2
- GRSPW2
- I2CMST
- SPICRTL

Filter:
- Parallel

Memory:
- FTHBRAM
- FTMCTRL
- MEMSCRUB
- SPIMCTRL

Processor:
- GPTIMER
- LEON3/LEON3FT

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NanoXplore new Major Software update NXmap v3 available now

NXmap is the main tool of NanoXplore design suite. It allows user to perform the design flow to program a FPGA including, synthesis, place, route, static timing analysis and bitstream generation. NXmap consists in a set of C++ libraries that can be controlled either through a graphic user interface or through a Python wrapper for scripting.
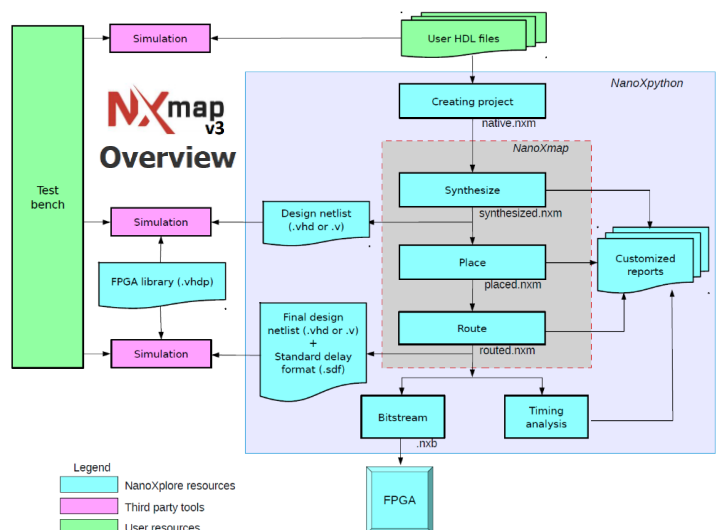
Features

nxmap and nxpython binaries are renamed in nxmap3 and nxpython3 respectively (links on old names are still present temporary) General improvement and enhancement of the full NXmap compilation algorithm.

GUI improvements:
- Add Home page
- New Create Project page
- New pads configuration page
- New Timing Analysis page
- New Inspector command
- New Aperture and Focus edit commands
- New constraints display page (synthesis and placement)
- Remarks, Warnings and Errors are displayed
- More tooltips added to give help inside tool
- New addDSPLocation() and addRAMLocation() method

Timing Analysis:
- Complete timing reports
- Timing constraints
- Timing analysis for PLL in NG-MEDIUM and NG-LARGE
- Limited maximum frequency for DSP, RAM and DFF
- Derating available for NG-MEDIUM and NG-LARGE: Best/Worst case analysis condition (voltage and temperature)
- Complete bitstream generation for NG-MEDIUM and NG-LARGE (EMBEDDED variants too)
- Simulator object available
- Adding documentation for progress method
- Python documentation updated

NXmap v3 Overview